Hardent
Quality Electronic Design Services

Trilogic

Advanced FPGA Design and Verification Flow Seminar Series
9:00 a.m. to 4:00 p.m. Wednesday September 19, 2012
St. Laurent, Quebec

Agenda

08:30 – 09:00	Registration
09:00 – 09:10	Welcome and Introduction
09:10 – 09:20	Why do you need a Verification Process
09:20 – 09:30	Three Steps to injecting Automation
09:30 – 10:00	Reduce debug Time by 50%
10:00 – 10:10	Break
10:10 – 10:40	Understand where you are in the Verification Process
10:40 – 11:15	Build an effective Testbench Infrastructure
11:15 – 12:00	The Vivado Design Flows
12:00 – 12:30	Lunch
12:30 – 13:30	Vivado Visualization capabilities
13:30 – 14:20	Xilinx design constraints (XDC) introduction
14:20 – 14:30	Break
14:30 – 15:00	Special consideration Signal Integrity for FPGA
15:00 – 15:20	BER Concern with DC Drop
15:20 – 15:40	AC Noise in Power Plane
15:40 – 16:00	Summary